

# Banc d'Essai de «Proof of Concept»

(D mo illustrant l'utilisation de la Synchronisation Verticale par Micka l P.)

Essais et texte de Andr  C.

Le support 'Hardware' de cette Synchronisation Verticale se r duit   un simple fil. Si cela est encore trop pour vous, vous pouvez utiliser Euphoric. En effet la touche F1 permet d'acc der   une simple option qu'il faut valider. Le programme de d mo est  crit en langage machine. Mais vous n'aurez pas besoin de vous pencher dessus si vous vous contentez d'admirer la d mo. Ce que je vous recommande, car ni l'illustration officielle (alpha ci-dessous), ni celles que j'ai ajout es ne laissent imaginer le r sultat. En effet, le programme 'trace'   l'ecran un point lumineux qui se d place dans les 3 dimensions. Les figures qui en r sultent et qui se retournent sur elles-m mes sont des plus fascinantes. L'utilisation des fl ches permet de changer les param tres et de varier les figures. Bon amusement!

Proof Of Concept #1

Double buffered sinus Dots @50hz

  2006 - Dbug

This is not really an intro in the demo scene usual definition of the term. There is no music and only one boring effect (sinus dots).

This is however a milestone in the ORIC demo history, because it shows for the first time a working real double buffer animation.

The picture that appear next indicates how to enable the hardware vsync. This is just a wire to connect between two connectors. Dumb simple, honest. (Recent emulators can emulate this)

== Press SPACE to continue ==

Hardware VSync  
Connection Diagram

RGB  
1-RED  
2-GREEN  
3-BLUE  
4-VSYNC  
5-GROUND

TAPE  
1-OUTPUT  
2-GROUND  
3-INPUT  
4-SOUND  
5-REMOTE

ORIC

Status of the VSYNC:  
== No input. Please connect Vsync ==

```

PRESET 00
BASE SPEED ALPHA X 01
BASE SPEED BETA X 00
SPEED ALPHA X +10
SPEED BETA X +00
BASE SPEED ALPHA Y 01
BASE SPEED BETA Y 01
SPEED ALPHA Y +10
SPEED BETA Y -2
    
```

```

PRESET 01
BASE SPEED ALPHA X 00
BASE SPEED BETA X 00
SPEED ALPHA X 00
SPEED BETA X 00
BASE SPEED ALPHA Y 00
BASE SPEED BETA Y 00
SPEED ALPHA Y 00
SPEED BETA Y 00
    
```

```

PRESET 02
BASE SPEED ALPHA X 00
BASE SPEED BETA X 00
SPEED ALPHA X 00
SPEED BETA X 00
BASE SPEED ALPHA Y 00
BASE SPEED BETA Y 00
SPEED ALPHA Y 00
SPEED BETA Y 00
    
```

```

PRESET 03
BASE SPEED ALPHA X 00
BASE SPEED BETA X 00
SPEED ALPHA X 00
SPEED BETA X 00
BASE SPEED ALPHA Y 00
BASE SPEED BETA Y 00
SPEED ALPHA Y 00
SPEED BETA Y 00
    
```

```

PRESET 04
BASE SPEED ALPHA X 00
BASE SPEED BETA X 00
SPEED ALPHA X 00
SPEED BETA X 00
BASE SPEED ALPHA Y 00
BASE SPEED BETA Y 00
SPEED ALPHA Y 00
SPEED BETA Y 00
    
```

```

PRESET 05
BASE SPEED ALPHA X 00
BASE SPEED BETA X 00
SPEED ALPHA X 00
SPEED BETA X 00
BASE SPEED ALPHA Y 00
BASE SPEED BETA Y 00
SPEED ALPHA Y 00
SPEED BETA Y 00
    
```

```

PRESET 06
BASE SPEED ALPHA X 00
BASE SPEED BETA X 00
SPEED ALPHA X 00
SPEED BETA X 00
BASE SPEED ALPHA Y 00
BASE SPEED BETA Y 00
SPEED ALPHA Y 00
SPEED BETA Y 00
    
```